RECENT DEVELOPMENT OF TRANSFERRED ELECTRON LOGIC DEVICES IN JAPAN

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Abstract

Recent progresses of TEDs in pulse processing applications in Japan are surveyed. Application to PCM transmission systems and ultra-high-speed logic systems are described as well as the ion-implanted TED, interfacial problems and the new material for lower dissipation power devices.

Introduction

In 1967, the application of the transferred electron (TE) effect to logic devices was proposed by several authors.[1] A complex current waveshape generator, an A-D convertor and some other logic devices were experimentally demonstrated by using a TED having a complex geometrical structure. Among them, a planar TE diode has been most extensively studied at Univ. of Tokyo, ETL, ECL, Fujitsu and NEC in Japan as well as in U.S.A., Germany and Great Britain for a pulse processing application.

This paper presents some topics on the recent remarkable progresses in TELDs in Japan.

Pulse Regeneration

An ultra-high-speed pulse regenerator may be the first place where a planar TELD can be applied, since the pulse re-shaping and regeneration are fundamental functions of the TE effect. The regeneration of ultra-high speed pulses are easily realized by the Schottky-Barrier-Gate Gunn-Effect-Digital Device (SBG-GEDD) with the simple circuit.[2] The PCM transmission system can be composed of simplified regenerative repeaters by interposing main repeaters with the retiming function as shown in the inset of Fig.1. The distance between main repeaters is mainly determined by the jitter time. The relation between the jitter time and the distance is reproduced for 1 Gbit/s rate system in Fig.1.[3] In the present PCM-400 Mbit system, the distance between two repeaters is 1.5 km. By employing simplified TE repeaters with 10 psec jitter, this distance can be expanded to 18Km in the 1 Gbit/s system. The SBG-GEDD can also simplify the re-timing and regeneration circuits in the conventional repeater.

For an optical fiber communication system in future, the SBG-GEDD can be employed as a direct modulator of a light source.[4] The waveshape of direct modulation of a laser diode is shown in Fig.2. The circuit is the series connection of an SBG-GEDD and a DH laser diode as illustrated in the inset. The signal pattern is [1110] with 500 Mbit rate. The upper trace shows the modulating current and the lower trace is the output voltage from the APD detector.

Logic System Application

In principle, a large logic system can be realized only with TELDs. However, the state of the art of GaAs technology is not advanced enough for achieving GaAs large scale integrated circuits. Therefore, the way to the application of TELDs is (1) to restrict the scale of the logic system to the simple one or (2) to make a sub-system of GaAs TELDs which determines the operating speed of the whole system of silicon devices.

As an example of the second case, Fujitsu developed an ultra-high-speed carry generator using the lateral spreading of a high field domain.[5] Since the velocity of the lateral spreading is very high ($1 - 2 \times 10^8$ cm/sec), the carry generator is expected to be operable at much higher speed than any conventional one. Fujitsu first demonstrated how to utilize the lateral spreading effect to a carry generator by computer simulation and succeeded in fabrication of the 4-stage ultra-high-speed generator. The device structure is shown in Fig.3. The operational principle is the following. The carry signal corresponds to the lateral spreading of a domain. This signal can be controlled by the ohmic gate, G. When the trigger pulse is applied to Schottky Gate, S_1, then the domain launches toward Anode A_1 and a negative pulse appears at A_1. If G_1 is off, namely, G_1 is kept at 13V, the domain can not spread to the second element and no signal appears at A_2, A_3 and A_4 as illustrated in the first left column of Fig.4. When voltage is increased by 0.5V at G_1, or G_1 is ON, the domain spreads to the second element and the signal appears at A_2 as shown in the second left column. The delay time in the 4-stage carry generator is 200 psec. When the Schottky gate is placed only in the first element, the delay time between the first and the fourth is 50ps as predicted by theory. A 4-bit full adder can be constructed by this type of carry generator and exclusive OR gates in Fig.5. The extension is possible to the longer word length system. In this case, the reduction of the addition time and the number of necessary active elements is remarkable in the Gunn-effect carry generator.

Fujitsu has also been investigating the integration of subsystems. For instance, Fig.6 illustrates the 2-bit dynamic shift register[6] which consists of 7 dual gate SBG-GEDDs[7] and 7 load resistors. Fig.7 shows the waveshapes. The middle trace is the input pulse. The output pulse comes out at A_2 just after 1 bit delay. Since the rise time and delay time are expected to be about 50 psec, the maximum clock rate will be 5 GHz. It should be noted that this GaAs integrated circuit was operated in DC bias condition.

Ion-Implanted SBG-GEDD and New Material for Lower Threshold Field

A planar GaAs device is usually fabricated by the epitaxial growth of a thin layer on a semi-insulating GaAs substrate. Since the active layer is thin (2-5 μm) and the substrate contains many deep centers, the effect of the interface between the layer and the substrate becomes important.

The anomalous effect is often observed in the anode current against voltage curves when the device is DC-biased.[8] The typical curves are shown in Fig.8. When the gate and anode bias voltages are pulsed, the I-V curves are normal(A). However, when the bias is given in DC, the current becomes smaller as shown in (B). This current reduction in the DC bias condition can be

interpreted by the model that the interfacial layer contains many empty deep states and injected electrons are trapped by these centers to form the negative space charge layer, which in turn modulates the current channel. The intensive study has been made about these effects to find the origin of this anomalous effect and to improve the interface properties. The same problem also arises in FETs. The effect was apparently reduced by the tetrode structure that has a subsidiary anode electrode[9].

One of the interesting attempts is to use ion implantation technique for fabrication of an active layer. Fig.9 shows the sulfur-implanted SBG-GEDD, which was fabricated by ECL.[10] Fig.10 illustrates the wave-shapes of this device successfully operated in a trigger mode at DC bias.

One of the disadvantages in logic application of a TED is rather high dissipation power. The lower limit is given by the threshold field of 3.2 kV/cm in GaAs. To make the lower dissipation power logic-device, a material with lower threshold field is desired. The first candidate is the ternary alloy of $Ga_xIn_{1-x}Sb$. The project team was organized by ETL to grow and characterize $Ga_xIn_{1-x}Sb$ and to fabricate TELD. Fig.11 shows typical Gunn oscillation with $Ga_xIn_{1-x}Sb$ (for x=0.4 to 0.87). The further study is needed to refine the crystal technology.

Conclusion

The recent development on the transferred electron devices was surveyed in pulse-processing systems. The key for TELDs to get out from the laboratory to the field is in the material and device technologies of GaAs. The problems arise from the interfacial properties between epitaxial layer and substrate, characteristics of Cr-doped substrates and the surface instability of planar devices.

A GaAs FET has similar structure and also can be operated at ultra-high-speed. The big difference is that the TE effect has itself pulse reshaping and threshold functions, while the FET is an analog amplifier. Thus, by using these advantages positively, TELDs and FETs can be employed complimentarily in ultra-high-speed electronic systems.

Acknowledgement

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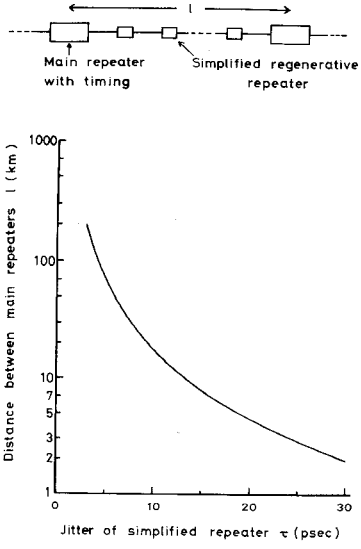


Fig.1. Main repeater interval as a function of jitter time of a simplified regenerative repeater.

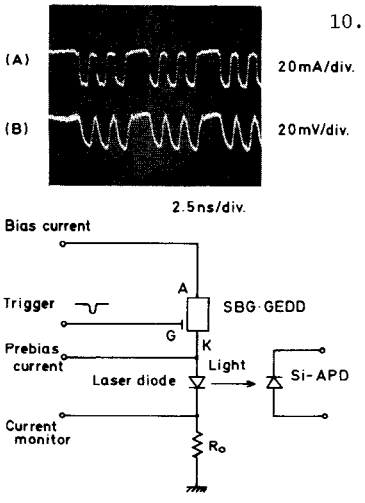


Fig.2. Direct modulation of a semi-conductor laser by using a SBG-GEDD at 500 Mbit/s
(A) drive-current pattern
(B) modulated light detected by a Si-Avalanche photodiode

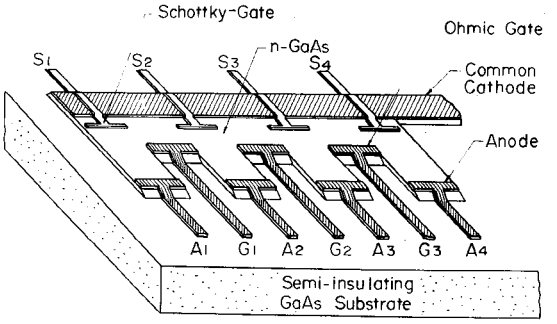


Fig.3. Schematic diagram of a 4-bit carry generator using the lateral spreading of a high field domain.

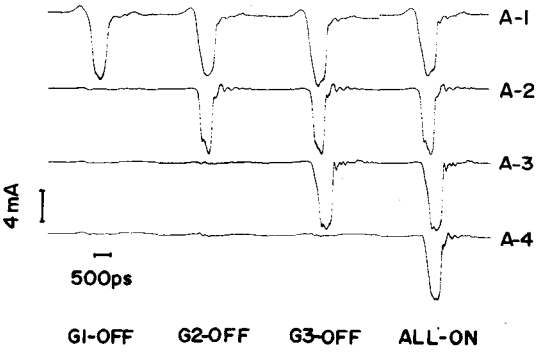


Fig.4. Output anode current at each element of the 4-bit carry generator.

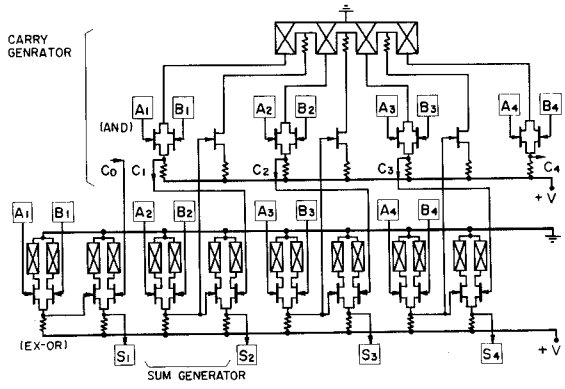


Fig.5. Full adder circuit composed of the Gunn-effect carry generator and FET-controlled Exclusive OR gates.

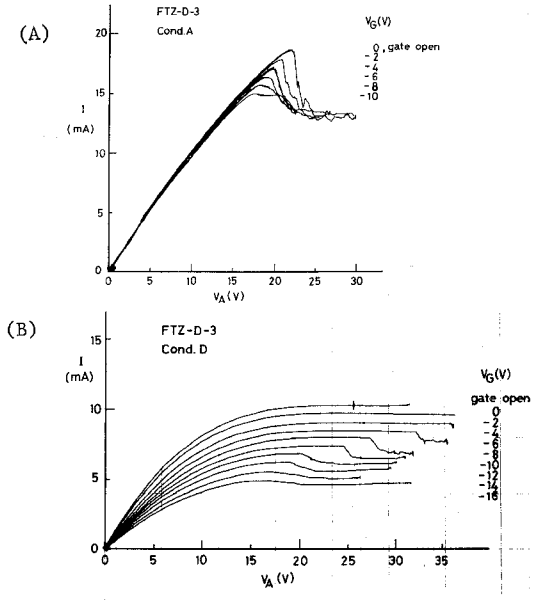


Fig.8. Typical I-V curves of a SBG-GEDD.
(A) pulse bias
(B) DC bias

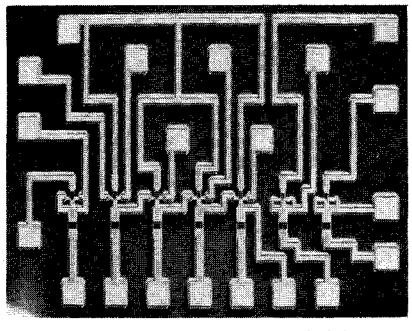


Fig.6. An integrated 2-bit shift register.

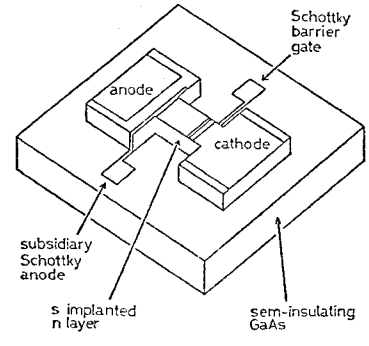


Fig.9. Schematic structure of a Sulfur-implanted SBG-GEDD.

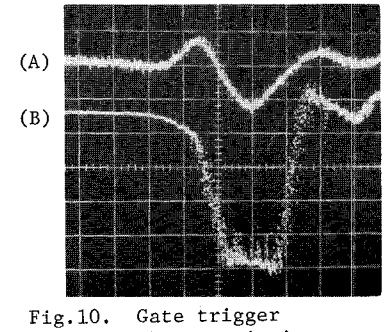


Fig.10. Gate trigger characteristics
(A) gate input voltage: 200mV/div.
(B) output current: 2mA/div.
Horizontal : 200 psec/div.

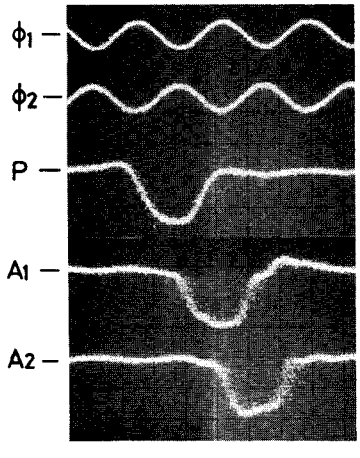
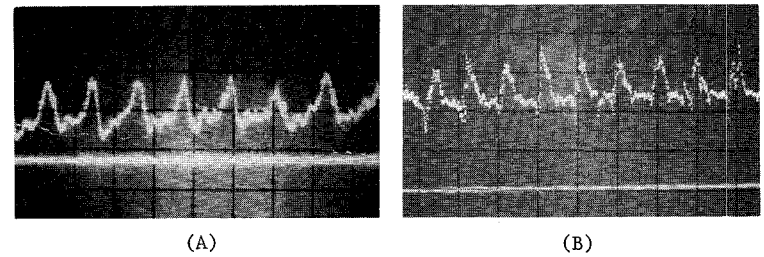


Fig.7. Operating waveforms of the shift register at the clock rate of 1.6 GHz.
ϕ_1, ϕ_2 : clock pulses
P : input pulse
A_1, A_2 : output pulses of the first two AND gates.



(A) (B)

Fig.11. Current waveform of free running oscillation in $Ga_xIn_{1-x}Sb$
(A) x=0.70, Vertical : 48 mA/div.
Horizontal : 2nsec/div.
(B) x=0.40, Vertical: 152 mA/div.
Horizontal : 4nsec/div.